x4

EXTRA TOPICS RELATED TO

# Output Stage and Power Amplifiers



This supplement contains material removed from previous editions of the textbook. These topics continue to be relevant and for this reason will be of great value to many instructors and students.

Specifically, the topics presented here extend the material presented in Chapter 12 of the eighth edition of the textbook. The material on the Class B output stage augments section 12.3 of the text. Device protection measures can be discussed along with the material in section 12.5 of the text. A classical CMOS class AB configuration could augment section 12.6 of the text. Section 12.7 describes power transistors and can be augmented with material on their thermal considerations presented here. Finally, the extra topic of IC power amplifiers can be used to further extend Chapter 12.

## x4.1 Crossover Distortion and Single-Supply Operation in the Class B Output Stage

### x4.1.1 Reducing Crossover Distortion

The crossover distortion of a class B output stage can be reduced substantially by employing a high-gain op amp and overall negative feedback, as shown in Fig. x4.1. The ±0.7-V dead band is reduced to $\pm 0.7/A_0$ volt, where $A_0$ is the dc gain of the op amp. Nevertheless, the slew-rate limitation of the op amp will cause the alternate turning on and off of the output transistors to be noticeable, especially at high frequencies. A more practical method for reducing and almost eliminating crossover distortion is found in the class AB stage, which we studied elsewhere.

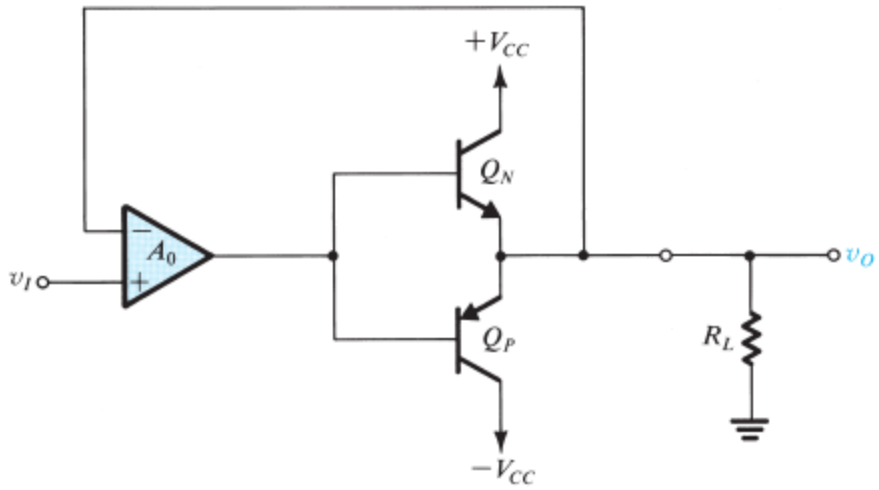


**Figure x4.1** Class B circuit with an op amp connected in a negative-feedback loop to reduce crossover distortion.

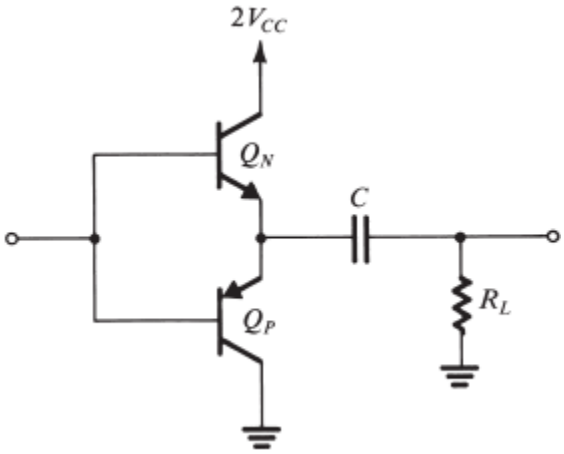


**Figure x4.2** Class B output stage operated with a single power supply.

### x4.1.2 Single-Supply Operation

The class B stage can be operated from a single power supply, in which case the load is capacitively coupled, as shown in Fig. x4.2. Note that to make the formulas derived in Section 12.3.4 of the textbook's eighth edition directly applicable, the single power supply is denoted $2V_{CC}$.

## x4.2 Device Protection Measures

### x4.2.1 Short-Circuit Protection

Figure x4.3 shows a class AB output stage equipped with protection against the effect of short-circuiting the output while the stage is sourcing current. The large current that flows through $Q_1$ in the event of a short circuit will develop a voltage drop across $R_{E1}$ of sufficient value to turn $Q_5$ on. The collector of $Q_5$ will then conduct most of the current $I_{BIAS}$, robbing $Q_1$ of its base drive. The current through $Q_1$ will thus be reduced to a safe operating level.

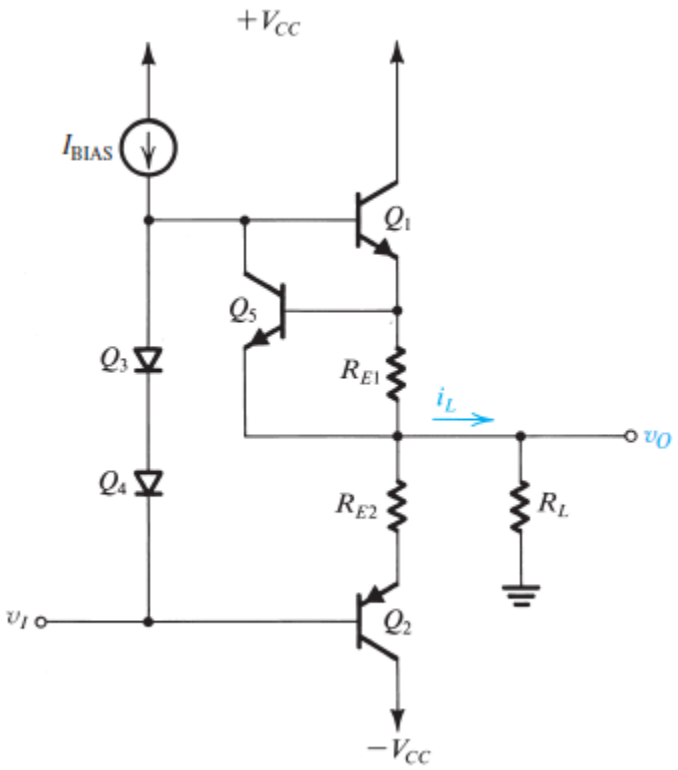


**Figure x4.3** A class AB output stage with short-circuit protection. The protection circuit shown operates in the event of an output short circuit while $v_O$ is positive.

This method of short-circuit protection is effective in ensuring device safety, but it has the disadvantage that under normal operation about 0.5 V drop might appear across each $R_E$. This means that the voltage swing at the output will be reduced by that much, in each direction. On the other hand, the inclusion of emitter resistors provides the additional benefit of protecting the output transistors against thermal runaway.

## EXERCISE

**xD4.1** In the circuit of Fig. x4.3 let $I_{BIAS} = 2$ mA. Find the value of $R_{E1}$ that causes $Q_5$ to turn on and absorb all 2 mA when the output current being sourced reaches 150 mA. For $Q_5$, $I_S = 10^{-14}$ A. If the normal peak output current is 100 mA, find the voltage drop across $R_{E1}$ and the collector current of $Q_5$.

**Ans.** 4.3 Ω; 430 mV; 0.3 μA

### x4.2.2 Thermal Shutdown

In addition to short-circuit protection, most IC power amplifiers are usually equipped with a circuit that senses the temperature of the chip and turns on a transistor in the event that the temperature exceeds a safe preset value. The turned-on transistor is connected in such a way that it absorbs the bias current of the amplifier, thus virtually shutting down its operation. Figure x4.4 shows a thermal-shutdown circuit. Here, transistor $Q_2$ is

normally off. As the chip temperature rises, the combination of the positive temperature coefficient of zener diode $Z_1$ and the negative temperature coefficient of $V_{BE1}$ causes the voltage at the emitter of $Q_1$ to rise. This in turn raises the voltage at the base of $Q_2$ to the point at which $Q_2$ turns on.

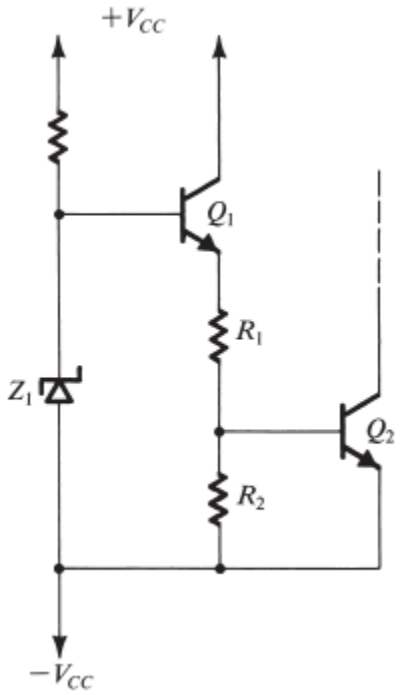


**Figure x4.4** Thermal-shutdown circuit.

## x4.3 A Classical Configuration of the CMOS Class AB Output Stage

Figure x4.5 shows the classical CMOS class AB output stage. The circuit is the exact counterpart of the bipolar circuit shown in Fig. 12.13 with the biasing diodes implemented with diode-connected transistors $Q_1$ and $Q_2$. The constant current $I_{\text{BIAS}}$ flowing through $Q_1$ and $Q_2$ establishes a dc bias voltage $V_{GG}$ between the gates of $Q_N$ and $Q_P$. This voltage in turn establishes the quiescent ($v_O = 0$) current $I_Q$ in $Q_N$ and $Q_P$. Unlike the BJT circuit in Fig. 12.13, here the zero dc gate current of $Q_N$ results in the current through $Q_1$ and $Q_2$ remaining constant at $I_{\text{BIAS}}$ irrespective of the value of $v_O$ and the load current $i_L$. Thus $V_{GG}$ remains constant and the circuit is more like the idealized bipolar case shown in Fig. 12.10.

We can find the value of $I_Q$ using the $i_D$–$v_{GS}$ equations for the four MOS transistors for the case $v_O = 0$. Neglecting channel-length modulation, we can write for $Q_1$,

$$I_{D1} = I_{\text{BIAS}} = \frac{1}{2}k_n'(W/L)_1(V_{GS1} - V_{tn})^2 \tag{x4.1}$$

and for $Q_2$,

$$I_{D2} = I_{\text{BIAS}} = \frac{1}{2} k_p'(W/L)_2 \left(V_{SG2} - V_{tp}\right)^2$$

(x4.2)

Equations (x4.1) and (x4.2) can be used to find $V_{GS1}$ and $V_{SG2}$, which when summed yield $V_{GG}$; thus,

$$V_{GG} = V_{GS1} + V_{SG2} = V_{tn} + |V_{tp}| + \sqrt{2I_{\text{BIAS}}} \left( \frac{1}{\sqrt{k_n'(W/L)_1}} + \frac{1}{\sqrt{k_p'(W/L)_2}} \right)$$

(x4.3)

We can follow a similar process for $Q_N$ and $Q_P$, which, for $v_O = 0$, are conducting the quiescent current $I_Q$; thus,

$$V_{GG} = V_{GSN} + V_{SGP} = V_{tn} + |V_{tp}| + \sqrt{2I_Q} \left( \frac{1}{\sqrt{k_n'(W/L)_n}} + \frac{1}{\sqrt{k_p'(W/L)_2}} \right)$$

(x4.4)

Equations (x4.3) and (x4.4) can be combined to obtain

$$I_Q = I_{\text{BIAS}} \left[ \frac{1/\sqrt{k_n'(W/L)_1} + 1/\sqrt{k_p'(W/L)_2}}{1/\sqrt{k_n'(W/L)_n} + 1/\sqrt{k_p'(W/L)_p}} \right]^2$$

(x4.5)

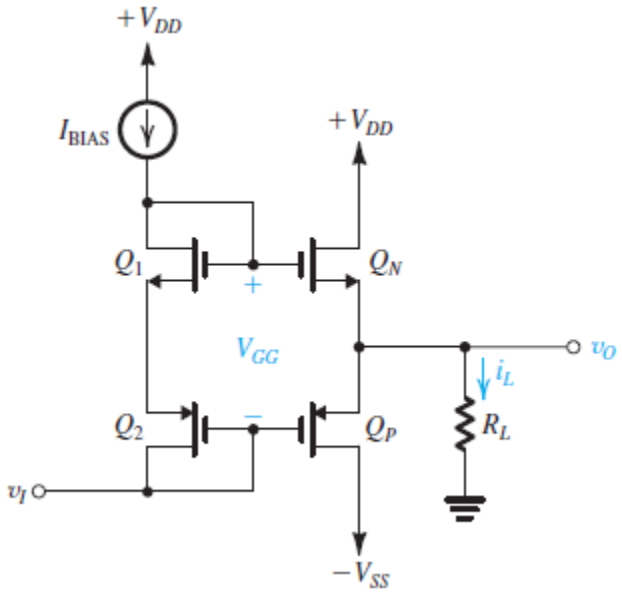


**Figure x4.5** Classical CMOS class AB output stage. This circuit is the CMOS counterpart of the BJT circuit in Fig. 12.13 with the biasing diodes implemented with diode-connected MOSFETs $Q_1$ and $Q_2$

which indicates that $I_Q$ is determined by $I_{\text{BIAS}}$ together with the $(W/L)$ ratios of the four transistors. For the case $Q_1$ and $Q_2$ are matched, that is,

$$k_p'(W/L)_2 = k_n'(W/L)_1 \tag{x4.6}$$

and $Q_N$ and $Q_P$ are matched, that is,

$$k_p'(W/L)_2 = k_n'(W/L)_1 \tag{x4.7}$$

Equation (x4.5) simplifies to

$$I_Q = I_{\text{BIAS}} \frac{(W/L)_n}{(W/L)_1} \tag{x4.8}$$

which is an intuitively appealing result.

## EXERCISE

**x4.2** For the CMOS class AB output stage of Fig. x4.5, consider the case of matched $Q_1$ and $Q_2$, and matched $Q_N$ and $Q_P$. If $I_Q$ = 1 mA and $I_{\text{BIAS}}$ = 0.2 mA, find $(W/L)$ for each of $Q_1$, $Q_2$, $Q_N$, and $Q_P$ so that in the quiescent state each transistor operates at an overdrive voltage of 0.2 V. Let $V_{DD} = V_{SS}$ = 2.5 V, $k'_n$ = 250 μA/V$^2$, $k'_p$ = 100 μA/V$^2$, and $V^{tn} = -V_{tp}$ = 0.5 V. Also find $V_{GG}$.

**Ans.** 40; 100; 200; 500; 1.4 V

A drawback of the CMOS class AB circuit of Fig. x4.5 is the restricted range of output voltage swing. To find the maximum possible value of $v_O$, refer to Fig. x4.5 and assume that across the bias current source is a dc voltage of $V_{\text{BIAS}}$. We can write for $v_O$,

$$v_O = V_{DD} - V_{\text{BIAS}} - v_{GSN} \tag{x4.9}$$

The maximum value of $v_O$ will be limited by the need to keep $V_{\text{BIAS}}$ to a minimum of $V_{OV}$ of the transistor supplying $I_{\text{BIAS}}$ (otherwise the current-source transistor no longer operates in saturation); thus,

$$v_{O\max} = V_{DD} - V_{DD} - V_{OV}|_{\text{BIAS}} - v_{GSN} \tag{x4.10}$$

Note that when $v_O$ is at its maximum value, $Q_N$ will be supplying most or all of $i_L$, and $v_{GSN}$ will be large, thus

$$v_{O\max} = V_{DD} - V_{OV}|_{\text{BIAS}} - V_{tn} - v_{OVN} \tag{x4.11}$$

where $v_{OVN}$ is the overdrive voltage of $Q_N$ when it is supplying $i_{L\max}$.

**EXERCISE**

**x4.3** For the circuit specified in Exercise x4.2, find $v_{O\max}$ when $i_{L\max}$ = 10 mA. Assume that $Q_N$ is supplying all of $i_{L\max}$ and that $V_{OV}|_{\text{BIAS}}$ = 0.2 V.

**Ans.** 1.17 V

The minimum allowed value of $v_O$ can be found in a similar way. Here we note that the transistor supplying vI (not shown) will need a minimum voltage across it of $V_{OV}|_I$. Thus,

$$v_{O\min} = -V_{SS} + V_{OV}|_I + |V_{tp}| + |v_{OVP}| \tag{x4.12}$$

where $|v_{OVP}|$ is the overdrive voltage of $Q_P$ when sinking the maximum negative value of $i_L$.

Finally, we observe that the reason for the lower allowable range of $v_O$ in the CMOS circuit is the relatively large value of $v_{OVN}$ and $|v_{OVP}|$; that is, the large values of $v_{GSN}$ and $v_{SGP}$ required to supply the large output currents. In the BJT circuit the corresponding voltages, $v_{BEN}$ and $v_{EBP}$, remain close to 0.7 V. The overdrive voltages $v_{OVN}$ and $|v_{OVP}|$ can be reduced by making the $W/L$ ratios of $Q_N$ and $Q_P$ large. This, however, can lead to impractically large devices.

## x4.4 Thermal Considerations in Power Transistors

Power transistors dissipate large amounts of power. The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature $T_J$ must not be allowed to exceed a specified maximum, $T_{J\max}$; otherwise the transistor could suffer permanent damage. For silicon devices, $T_{J\max}$ is in the range of 150°C to 200°C.

### x4.5.1 Thermal Resistance

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor will be conducted away from the junction to the transistor case, and from the case to the surrounding environment. In a steady state in which the transistor is dissipating $P_D$ watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

$$T_J - T_A = \theta_{JA} P_D \tag{x4.13}$$

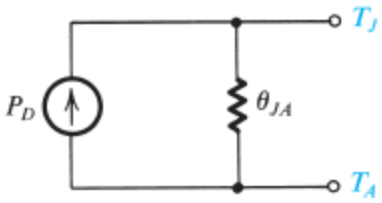


**Figure x4.6** Electrical equivalent circuit of the thermal conduction process; $T_J - T_A = P_D\theta_{JA}$.

where $\theta_{JA}$ is the **thermal resistance** between junction and ambience, having the units of degrees Celsius per watt. Note that $\theta_{JA}$ simply gives the rise in junction temperature over the ambient temperature for each watt of dissipated power. Since we wish to be able to dissipate large amounts of power without raising the junction temperature above $T_{J\max}$, it is desirable to have, for the thermal resistance $\theta_{JA}$, as small a value as possible. For operation in free air, $\theta_{JA}$ depends primarily on the type of case in which the transistor is packaged. The value of $\theta_{JA}$ is usually specified on the transistor data sheet.

Equation (x4.13), which describes the thermal-conduction process, is analogous to Ohm's law, which describes the electrical-conduction process. In this analogy, power dissipation corresponds to current, temperature difference corresponds to voltage difference, and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal-conduction process by the electric circuit shown in Fig. x4.6.

## x4.5.2 Power Dissipation versus Temperature

The transistor manufacturer usually specifies the maximum junction temperature $T_{J\max}$, the maximum allowable power dissipation at a particular ambient temperature $T_{A0}$ (usually 25°C), and the thermal resistance $\theta_{JA}$. In addition, a graph such as that shown in Fig. x4.7 is usually provided. The graph simply states that for operation at ambient temperatures below $T_{A0}$, the device can safely dissipate the rated value of $P_{D0}$ watts. However, if the device is to be operated at higher ambient temperatures, the maximum allowable power dissipation must be **derated** according to the straight line shown in Fig. x4.7. The **power-derating curve** is a graphical representation of Eq. (x4.13). Specifically, note that if the ambient temperature is $T_{A0}$ and the power dissipation is at the maximum allowed ($P_{D0}$), then the junction temperature will be $T_{J\max}$. Substituting these quantities in Eq. (x4.13) results in

$$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} \tag{x4.14}$$

which is the inverse of the slope of the power-derating straight line. At an ambient temperature $T_A$, higher than $T_{A0}$, the maximum allowable power dissipation $P_{D\max}$ can be obtained from Eq. (x4.13) by substituting $T_J = T_{J\max}$; thus,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} \tag{x4.15}$$

Observe that as $T_A$ approaches $T_{J\max}$, the allowable power dissipation decreases; the lower thermal gradient limits the amount of heat that can be removed from the junction. In the extreme situation of $T_A = T_{J\max}$, no power can be dissipated because no heat can be removed from the junction.

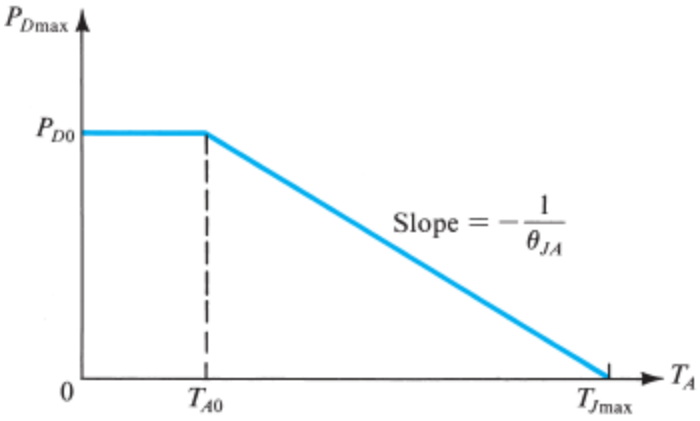


**Figure x4.7** Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a "power-derating" curve.

## Example x4.1

A BJT is specified to have a maximum power dissipation $P_{D0}$ of 2W at an ambient temperature $T_{A0}$ of 25°C, and a maximum junction temperature $T_{J\max}$ of 150°C. Find the following:

(a) the thermal resistance $\theta_{JA}$

(b) the maximum power that can be safely dissipated at an ambient temperature of 50°C

(c) the junction temperature if the device is operating at $T_A$ = 25°C and is dissipating 1W

**Solution**

(a) $\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} = \frac{150-25}{2} = 62.5°\text{C/W}$

(b) $P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150-50}{62.5} = 1.6\ \text{W}$

(c) $T_J = T_A + \theta_{JA}P_D = 25 + 62.5 \times 1 = 87.5°\text{C}$

### x4.5.3 Transistor Case and Heat Sink

The thermal resistance between junction and ambience, $\theta_{JA}$, can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \tag{x4.16}$$

where $\theta_{JA}$ is the thermal resistance between junction and transistor case (package) and $\theta_{CA}$ is the thermal resistance between case and ambience. For a given transistor, $\theta_{JC}$ is fixed by the device design and packaging. The device manufacturer can reduce $\theta_{JC}$ by encapsulating the device in a relatively large metal case, such as that in Fig. 12.25(a), and placing the collector (where most of the heat is dissipated) in direct contact with the case.

Although the circuit designer has no control over $\theta_{JC}$ (once a particular transistor has been selected), the designer can considerably reduce $\theta_{CA}$ below its free-air value (specified by the manufacturer as part of $\theta_{JA}$). Reduction of $\theta_{CA}$ can be effected by providing means to facilitate heat transfer from case to ambience. A popular approach is to bolt the transistor to the chassis or to an extended metal surface such as the heat sink shown in Fig. 12.26 of the textbook. Heat is easily conducted from the transistor case to the heat sink; that is, the thermal resistance $\theta_{CS}$ is usually very small. Also, heat is efficiently transferred (by convection and radiation) from the heat sink to the ambience, resulting in a low thermal resistance $\theta_{SA}$. Thus, if a heat sink is utilized, the case-to-ambience thermal resistance given by

$$\theta_{CA} = \theta_{CS} + \theta_{SA} \tag{x4.17}$$

can be small because its two components can be made small by the choice of an appropriate heat sink. For example, in very high-power applications the heat sink is usually equipped with fins that further facilitate cooling by radiation and convection.

The electrical analog of the thermal-conduction process when a heat sink is employed is shown in Fig. x4.8, from which we can write

$$T_J - T_A = P_D(\theta_{JC} = \theta_{CS} + \theta_{SA}) \tag{x4.18}$$

As well as specifying $\theta_{JC}$, the device manufacturer usually supplies a derating curve for $P_{D\max}$ versus the case temperature, $T_C$. Such a curve is shown in Fig. x4.9. Note that the slope of the power-derating straight line is $-1/\theta_{JC}$. For a given transistor, the maximum power dissipation at a case temperature $T_{C0}$ (usually 25°C) is much greater than that at an ambient temperature $T_{A0}$ (usually 25°C, because $\theta_{JC} \ll \theta_{JA}$). If the device can be maintained at a case temperature $T_C$, $T_{C0} \leq T_C \leq T_{J\max}$, then the maximum safe power dissipation is obtained when $T_J = T_{J\max}$,

$$P_{D\max} = \frac{T_{J\max} - T_C}{\theta_{JC}} \tag{x4.19}$$

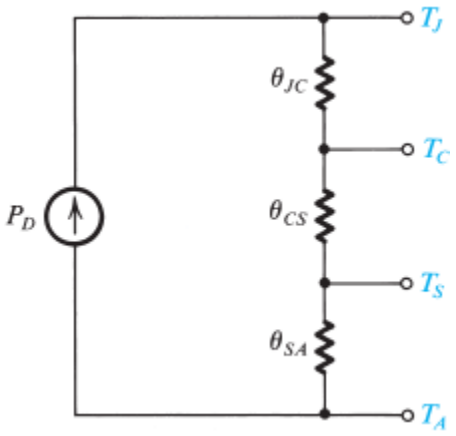


**Figure x4.8** Electrical analog of the thermal-conduction process when a heat sink is utilized.

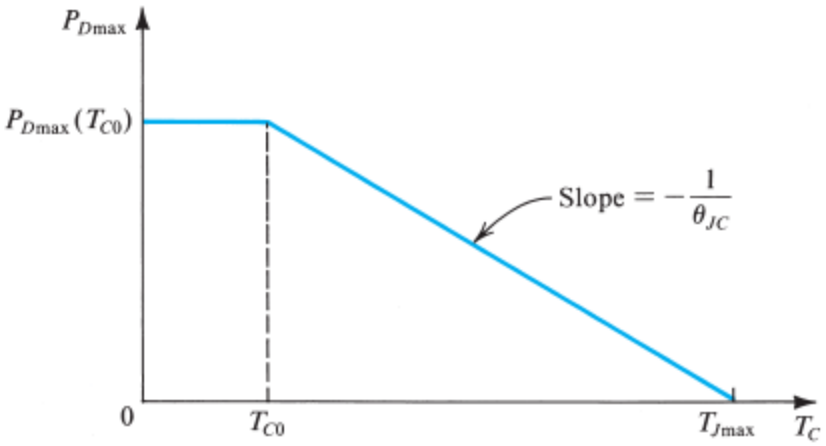


**Figure x4.9** Maximum allowable power dissipation versus transistor-case temperature.

## Example x4.2

A BJT is specified to have $T_{J\max}$ = 150°C and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_C = 25°\text{C}$$

$$2 \text{ W at } T_A = 25°\text{C}$$

Above 25°C, the maximum power dissipation is to be derated linearly with $\theta_{JC}$ = 3.12°C/W and $\theta_{JA}$ = 62.5°C/W. Find the following:

(a) The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A$ = 50°C.

(b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which $\theta_{CS}$ = 0.5°C/W and $\theta_{SA}$ = 4°C/W. Find the temperature of the case and of the heat sink.

(c) The maximum power that can be dissipated safely if an *infinite heat sink* is used and $T_A$ = 50°C.

**Solution**

(a)

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

(b) With a heat sink, $\theta_{JA}$ becomes

$$\begin{aligned}\theta_{JA} &= \theta_{JC} + \theta_{CS} + \theta_{CA} \\ &= 3.12 + 0.5 + 4.0 = 7.62°\text{C/W}\end{aligned}$$

Thus,

$$P_{D\max} = \frac{150 - 50}{7.62} = 13.1 \text{ W}$$

Figure x4.10 shows the thermal equivalent circuit with the various temperatures indicated.

(c) An infinite heat sink, if it existed, would cause the case temperature $T_C$ to equal the ambient temperature $T_A$. The infinite heat sink has $\theta_{CA} = 0$. Obviously, one cannot buy an infinite heat sink; nevertheless, this terminology is used by some manufacturers to describe the power-derating curve of Fig. x4.9. The abscissa is then labeled $T_A$ and the curve is called "power dissipation versus ambient temperature with an infinite heat sink." For our example, with infinite heat sink,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC}} = \frac{150 - 50}{3.12} = 32 \text{ W}$$

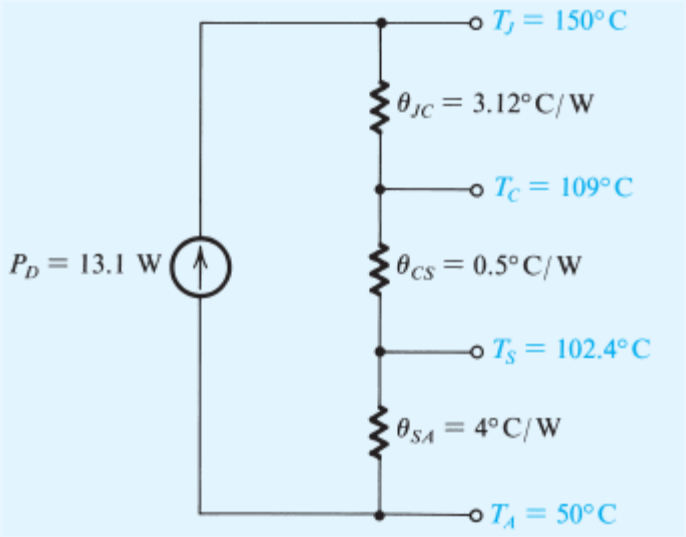


**Figure x4.10** Thermal equivalent circuit for Example x4.2

The advantage of using a heat sink is clearly evident from Example x4.2: With a heat sink, the maximum allowable power dissipation increases from 1.6W to 13.1 W. Also note that although the transistor considered can be called a "40-W transistor," this level of power dissipation cannot be achieved in practice; that would require an infinite heat sink and an ambient temperature $T_A \leq 25°C$.

**EXERCISE**

**x4.4** The 2N6306 power transistor is specified to have $T_{J\max} = 200°C$ and $P_{D\max} = 125W$ for $T_C \leq 25°C$. For $T_C \geq 25°C$, $\theta_{JC} = 1.4°C/W$. If in a particular application this device is to dissipate 50W and operate at an ambient temperature of 25°C, find the maximum thermal resistance of the heat sink that must be used (i.e., $\theta_{SA}$). Assume $\theta_{CS} = 0.6°C/W$. What is the case temperature, TC?

**Ans.** 1.5°C/W; 130°C

## x4.5 IC Power Amplifiers

A variety of IC power amplifiers are available. Most consist of a high-gain, small-signal amplifier followed by a class AB output stage. Some have overall negative feedback already applied, resulting in a fixed closed-loop voltage gain. Others do not have on-chip feedback and are, in effect, op amps with large output-power capability. In fact, the output current-driving capability of any general-purpose op amp can be increased by cascading it with a class B or class AB output stage and applying overall negative feedback. The additional output stage can be either a discrete circuit or a hybrid IC implementing, for example, the buffer in Fig. 12.16. In the following we discuss some power-amplifier examples.

**EARLY POWER-OP-AMP PRODUCT**

In 1985 Robert J. Widlar (1937–1991) and Mineo Yamatake at National Semiconductor introduced the LM12, probably the first very-high-power monolithic operational amplifier, offering an order-of-magnitude improvement over its predecessors. Nominally rated at 150-W output, this op amp could sustain 90W of continuous sine-wave output with a 40-Ω load, while handling up to 800W of short-term dynamic loading. The design operated from ±35-V supplies to provide a ±25-V signal with a ±10-A output. This monolithic amplifier employed polycrystalline film resistors for thermal stability. It incorporated a variety of novel protection features involving disconnection of the load from the output terminal, turn-on delay while awaiting internal stabilization, overtemperature control, and output-current limiting. It was internally unity-gain compensated with a unity-gain bandwidth of 700 kHz. While now obsolete, the LM12 was a clear forerunner of a modern approach to a vast array of special applications in audio and motor control.

### x4.4.1 A Fixed-Gain IC Power Amplifier

Our first example is the LM380 (a product of National Semiconductor Corporation), which is a fixed-gain monolithic power amplifier. A simplified version of the internal circuit of the amplifier is shown in Fig. x4.11. The circuit consists of an input differential amplifier utilizing $Q_1$ and $Q_2$ as emitter followers for input buffering, and $Q_3$ and $Q_4$ as a differential pair with an emitter resistor $R_3$. The two resistors $R_4$ and $R_5$ provide dc paths to ground for the base currents of $Q_1$ and $Q_2$, thus enabling the input signal source to be capacitively coupled to either of the two input terminals.

The differential amplifier transistors $Q_3$ and $Q_4$ are biased by two separate currents: $Q_3$ is biased by a current from the dc supply $V_S$ through the diode-connected transistor $Q_{10}$, and resistor $R_1$; $Q_4$ is biased by a dc current from the output terminal through $R_2$. Under quiescent conditions (i.e., with no input signal applied) the two bias currents will be equal, and the current through and the voltage across $R_3$ will be zero. For the emitter current of $Q_3$ we can write

$$I_3 \simeq \frac{V_S - V_{EB10} - V_{EB3} - V_{EB1}}{R_1}$$

where we have neglected the small dc voltage drop across $R_4$. Assuming, for simplicity, all $V_{EB}$ to be equal,

$$I_3 \simeq \frac{V_S - 3V_{EB}}{R_1} \tag{x4.20}$$

For the emitter current of $Q_4$ we have

$$I_4 = \frac{V_O - V_{EB4} - V_{EB2}}{R_2} \simeq \frac{V_O - 2V_{EB}}{R_2} \tag{x4.21}$$

where $V_O$ is the dc voltage at the output, and we have neglected the small drop across $R_5$.

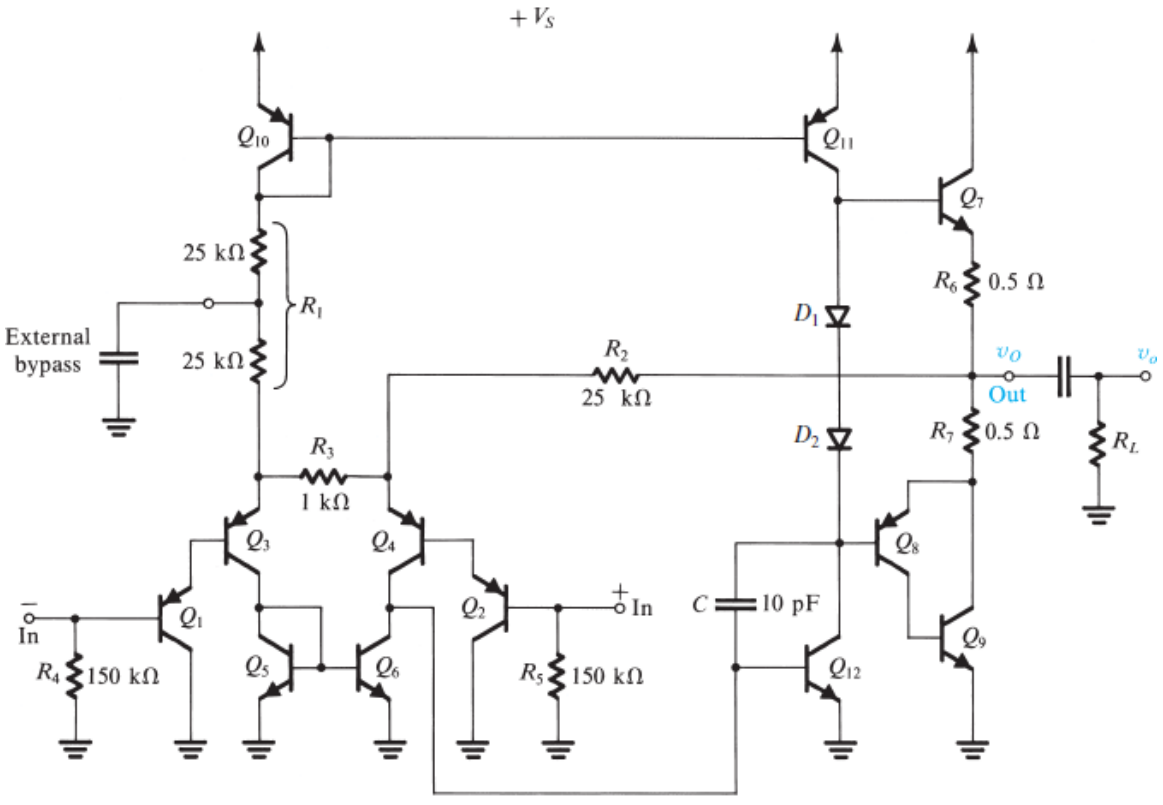


**Figure x4.11** The simplified internal circuit of the LM380 IC power amplifier. (Courtesy National Semiconductor Corporation.)

Equating $I_3$ and $I_4$ and using the fact that $R_1 = 2R_2$ results in

$$V_O = \frac{1}{2}V_S + \frac{1}{2}V_{EB} \tag{x4.22}$$

Thus the output is biased at approximately half the power-supply voltage, as desired for maximum output voltage swing. An important feature is the dc feedback from the output to the emitter of $Q_4$, through $R_2$. This dc feedback acts to stabilize the output dc bias voltage at the value in Eq. (x4.22). Qualitatively, the dc feedback functions as follows: If for some reason $V_O$ increases, a corresponding current increment will flow through $R_2$ and into the emitter of $Q_4$. Thus the collector current of $Q_4$ increases, resulting in a positive increment in the voltage at the base of $Q_{12}$. This, in turn, causes the collector current of $Q_{12}$ to increase, thus bringing down the voltage at the base of $Q_8$ and hence $V_O$.

Continuing with the description of the circuit in Fig. x4.11, we observe that the differential amplifier ($Q_3$, $Q_4$) has a current-mirror load composed of $Q_5$ and $Q_6$ (refer to Chapter 9, Section 9.5). The single-ended output voltage signal of the first stage appears at the collector of $Q_6$ and thus is applied to the base of the second-stage common-emitter amplifier $Q_{12}$. Transistor $Q_{12}$ is biased by the constant-current source $Q_{11}$, which also acts as its active load. In actual operation, however, the load of $Q_{12}$ will be dominated by the reflected resistance due to $R_L$. Capacitor $C$ provides frequency compensation (see Chapter 11).

The output stage is class AB, utilizing a compound *pnp* transistor ($Q_8$ and $Q_9$). Negative feedback is applied from the output to the emitter of $Q_4$ via resistor $R_2$. To find the closed-loop gain consider the small-signal equivalent circuit shown in Fig. x4.12. Here, we have replaced the second-stage common-emitter amplifier and the output stage with an inverting amplifier block with gain $A$.Weshall assume that the amplifier $A$ has high gain and high input resistance, and thus the input signal current into $A$ is negligibly small. Under this assumption, Fig. x4.12 shows the analysis details with an input signal $v_i$ applied to the inverting input terminal. The order of the analysis steps is indicated by the circled numbers. Note that since the input differential amplifier has a relatively large resistance, $R_3$, in the emitter circuit, most of the applied input voltage appears across $R_3$. In other words, the signal voltages across the emitter–base junctions of $Q_1$, $Q_2$, $Q_3$, and $Q_4$ are small in comparison to the voltage across $R_3$. Accordingly, the voltage gain can be found by writing a node equation at the collector of $Q_6$:

$$\frac{v_i}{R_3} + \frac{v_o}{R_2} + \frac{v_i}{R_3} = 0$$

which yields

$$\frac{v_o}{v_i} = -\frac{2R_2}{R_3} \simeq -50 \text{ V/V}$$

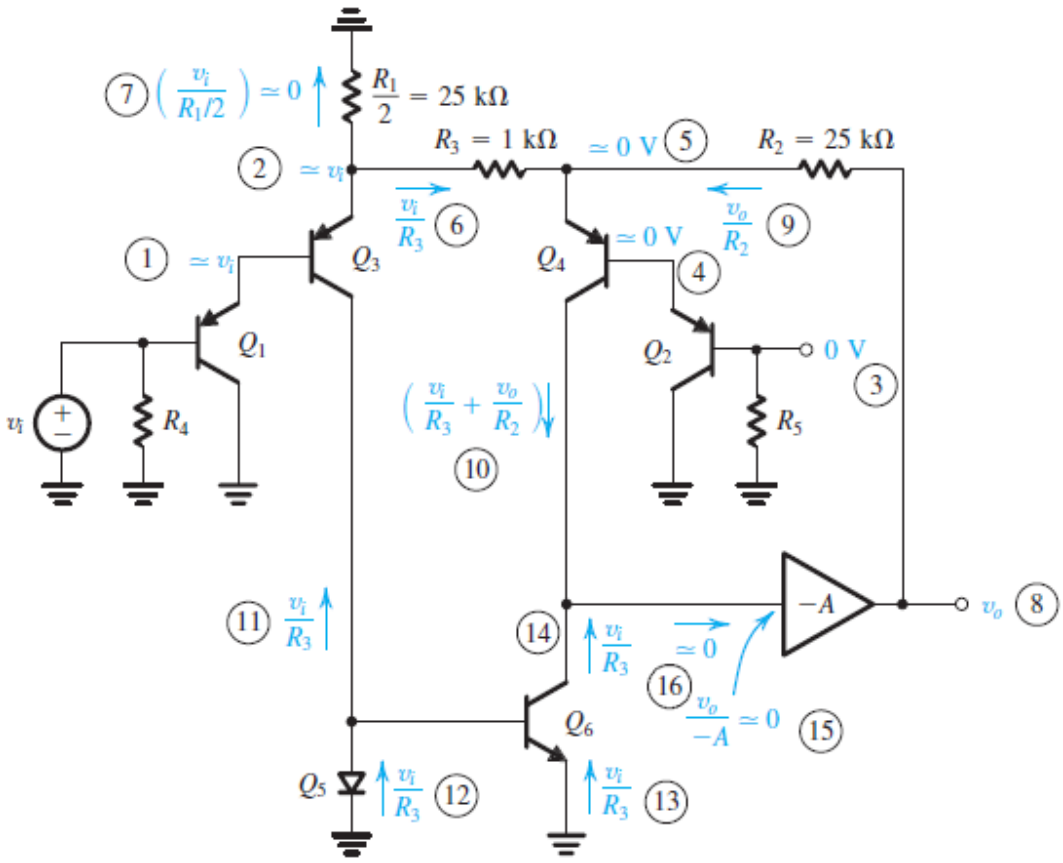


**Figure x4.12** Small-signal analysis of the circuit in Fig. x4.11. The circled numbers indicate the order of the analysis steps.

## EXERCISE

**x4.5** Denoting the total resistance between the collector of $Q_6$ and ground by $R$, show, using Fig. x4.12, that

$$\frac{v_o}{v_i} = \frac{-2R_2/R_3}{1 + (R_2/AR)}$$

which reduces to $(-2R_2/R_3)$ under the condition that $AR \gg R_2$.

As we demonstrated in Chapter 11, one of the advantages of negative feedback is the reduction of nonlinear distortion. This is the case in the circuit of the LM380.

The LM380 is designed to operate from a single supply $V_S$ in the range of 12 V to 22 V. The selection of supply voltage depends on the value of $R_L$ and the required output power $P_L$. The manufacturer supplies curves for the device power dissipation versus output power for a given load resistance and various supply voltages. One such set of curves for $R_L = 8\Omega$ is shown in Fig. x4.13. Note the similarity to the class B power dissipation curve of Fig. 12.9. In fact, you can easily verify that the location and value of

the peaks of the curves in Fig. x4.13 are accurately predicted by Eq. (12.21) in the textbook (where $V_{CC} = \frac{1}{2}V_S$). The line labeled "3% distortion level" in Fig. x4.13 is the locus of the points on the various curves at which the distortion (THD) reaches 3%. A THD of 3% represents the onset of peak clipping due to output-transistor saturation.

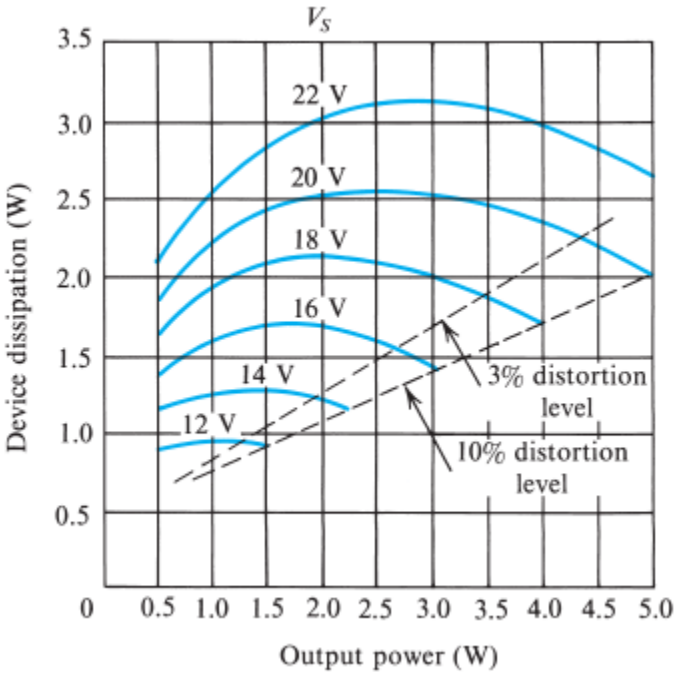


**Figure x4.13** Power dissipation ($P_D$) versus output power ($P_L$) for the LM380 with $R_L$ =8 Ω. (Courtesy National Semiconductor Corporation.)

## EXERCISE

**xD4.6** We are required to use the LM380 to drive an 8-Ω loudspeaker. Use the curves of Fig. x4.13 to determine the maximum power supply possible while limiting the maximum power dissipation to 2.9 W. If for this application a 3% THD is allowed, find $P_L$ and the peak-to-peak output voltage.

**Ans.** 20 V; 4.2 W; 16.4 V

### x4.4.2 The Bridge Amplifier

We conclude this section with a discussion of a circuit configuration that is popular in high-power applications. This is the bridge amplifier configuration shown in Fig. x4.14 utilizing two power op amps, $A_1$ and $A_2$. While $A_1$ is connected in the noninverting configuration with a gain $K = 1 + (R_2/R_1)$, $A_2$ is connected as an inverting amplifier with a gain of equal magnitude $K = R_4/R_3$. The load $R_L$ is floating and is connected between the output terminals of the two op amps.

If $v_I$ is a sinusoid with amplitude $\hat{V}_i$, the voltage swing at the output of each op amp will be $\pm K\hat{V}_i$, and that across the load will be $\pm 2K\hat{V}_i$. Thus, with op amps operated from ±15-V supplies and capable of providing, say, a ±12-V output swing, an output swing of ±24 V can be obtained across the load of the bridge amplifier.

In designing bridge amplifiers, note should be taken of the fact that the peak current drawn from each op amp is $2K\hat{V}_i/R_L$. This effect can be taken into account by considering the load seen by each op amp (to ground) to be $R_L/2$.

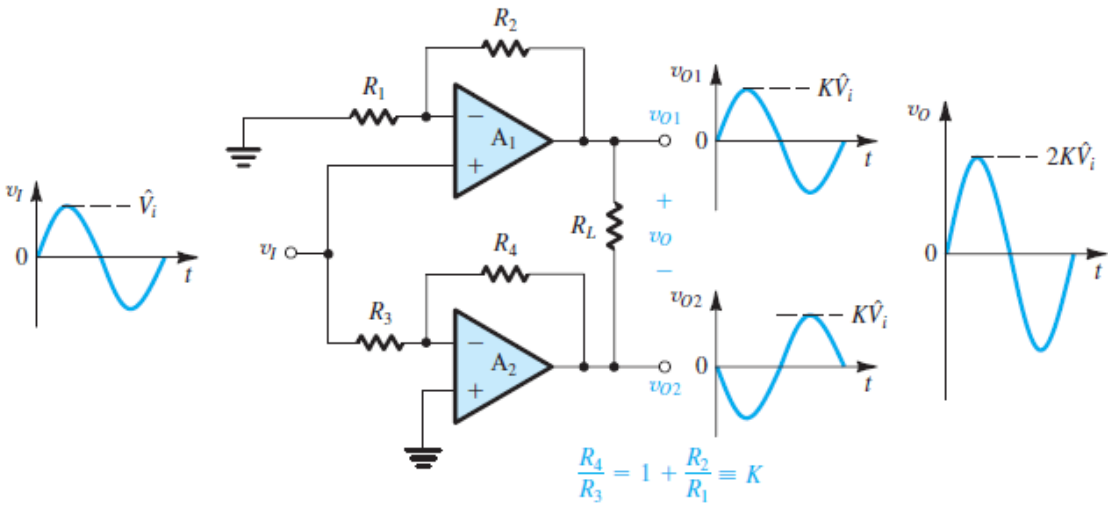


**Figure x4.14** The bridge amplifier configuration.

## EXERCISE

**x4.7** Consider the circuit of Fig. x4.14 with $R_1 = R_3 = 10$ kΩ, $R_2 = 5$ kΩ, R4 =15 kΩ, and $R_L = 8\Omega$. Find the voltage gain and the input resistance. The power supply used is ±18 V. If $v_I$ is a 20-V peak-to-peak sine wave, what is the peak-to-peak output voltage? What is the peak load current? What is the load power?

**Ans.** 3 V/V; 10 kΩ; 60 V; 3.75 A; 56.25W